IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 11. (Cancelled)

12. (Original) A semiconductor integrated circuit device including a well of a first conductivity type formed on a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate over a second insulator film and a third gate formed and isolated from said first gate through a third insulator film , wherein:

an upper surface of said third gate exists at a position lower than the upper surface of said first gate.

13. (Original) A semiconductor integrated circuit device according to claim 12, which has any of the following constructions:

a first construction wherein said first gate is a floating gate, said second gate is a control gate and said third gate is an erase gate;

a second construction wherein said first gate is a floating gate, said second gate is a control gate and said third gate is a gate for controlling a split channel; and

a third construction wherein said first gate is a floating gate, said second gate is a control gate and said third gate is a gate having the functions of both erase gate and gate for controlling a split channel.

14. (Original) A semiconductor integrated circuit device according to claim 13, wherein a part of said third gate exists over said semiconductor region of the second conductivity type.

15. (Original) A semiconductor integrated circuit device according to claim 12, wherein said first gate is a floating gate, said second gate is a control gate and said third gate is an erase gate; and

an entire surface of said third gate exists over said semiconductor region of the second conductivity type.

16. (Original) A semiconductor integrated circuit device according to claim 12, wherein said third insulator film is a silicon oxide film doped with nitrogen.

17. (Original) A semiconductor integrated circuit device including a well of a first conductivity type formed on a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film and a third gate formed and isolated from said first gate through a third insulator film, wherein;

said third gate has functions of both erase gate and gate for controlling a split channel.

18. (Original) A semiconductor integrated circuit device according to claim 17, wherein said third insulator film is a silicon oxide film doped with nitrogen.

19. (Original) A semiconductor integrated circuit device including a well of a first conductivity type formed on a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film and a third gate formed and isolated from said first gate through a third insulator film, wherein:

a film thickness of said first insulator film is greater than that of said second or third insulator film.

20. (Original) A semiconductor integrated circuit device including a well of a first conductivity type formed on a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film and third gate formed and isolated from said first gate through a third insulator film, wherein:

said second gate comprises a stacked film of a polysilicon film and a metal silicide film, and said third gate exists as it is buried into a space between said first gates.

21. (Original) A semiconductor integrated circuit device according to claim 20, wherein said metal silicide film is a tungsten film.

22. (Original) A semiconductor integrated circuit device according to claim 20, which has any of the following constructions:

a first construction wherein the space between said first gates is defined by end faces of said first gates parallel to the extending direction of said second gate among the end faces of said first gates; and

a second construction wherein the space between said first gates is defined by end faces of said first gates vertical to the extending direction of said second gate among the end faces of said first gates.

23. (Original) A semiconductor integrated circuit device including a well of a first conductivity type formed on a main surface of a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, a first gate formed over said semiconductor substrate through a first insulator film, a second gate formed over said first gate through a second insulator film and a third gate formed and isolated from said first gate through a third insulator film, wherein:

said second gate comprises a stacked film containing a metal film.

24. (Original) A semiconductor integrated circuit device according to claim 23, wherein said second gate comprises

a stacked film of a polysilicon film, a barrier metal film and a metal film.

25. (Original) A semiconductor integrated circuit device according to claim 23, wherein said third gate exists as it is buried into the space between said first gates.

26. (Original) A semiconductor integrated circuit device according to claim 23, which as any of the following constructions:

a first construction wherein the space between said first gates is defined by end faces of said first gates parallel to the extending direction of said second gates among the end faces of said first gates; and

a second construction wherein the space between said first gates is defined by end faces of said first gates vertical to the extending direction of said second gates among the end faces of said first gates.

27. (Original) A semiconductor integrated circuit device according to claim 24, wherein said barrier metal film belongs to a group of a tungsten film, a titanium film, a tantalum film, a metal film made of a transition metal itself or its nitride film or its silicide film, an aluminum nitride film, a cobalt silicide film, a molybdenum silicide film, a titanium tungsten film or their alloy films.

28. (Original) A semiconductor integrated circuit device according to claim 25, which has any of the following constructions:

a first construction wherein the space between said first gates is defined by end faces of said first gates parallel to the extending direction of said second gates among the end faces of said first gates; and

a second construction wherein the space between said first gates is defined by end faces of said first gates vertical to the extending direction of said second gates among the end faces of said first gates.

29. (Original) A semiconductor integrated circuit device including a well of a first conductivity type formed in a semiconductor substrate, a semiconductor region of a second conductivity type formed inside said well, local source lines and local

data lines formed by connecting said semiconductor region, select transistors for selecting said local source line and said local data lines, a first gate formed over said semiconductor integrated substrate through a first insulator film, a second gate formed and isolated from said first gate through a second insulator film, word lines formed by connecting said second gates, and a third gate formed and isolated from said first gate through a third insulator film and having different functions from said first and second gates and, wherein:

a bundling portion of said third gates exists between said word line existing at the nearest position to said select transistor inside a memory cell block comprising said select transistors and the gate of said select transistor.

30. (Original) A semiconductor integrated circuit device according to claim 29, wherein a dummy gate exists between said bundling portion of said third gates and said word line existing at the nearest position to said select transistor inside said memory cell block.

31. (Original) A semiconductor integrated circuit device according to claim 20, which has any of the following constructions:

a first construction wherein all of said third gates existing inside said memory cell are bundled at either one, or both of the ends of said memory cell block end; and

a second construction wherein every other of said third gates existing inside said memory cell block are bundled at the memory cell block end.

32. (Original) A semiconductor integrated circuit device according to claim 29, wherein all of said third gates existing inside said memory cell block are bundled

at either one, or both, of the ends of said memory cell block, and wherein the selection signal of said third gate is generated from a selection signal of said memory cell block.

33. (Original) A semiconductor integrated circuit device according to claim 29, wherein all of said third gates existing inside said memory cell block are bundled at either one, or both, of the ends of said memory cell block, said integrated circuit device having any of the following construction:

a first construction wherein the selection signal of said third gate is generated from a selection signal of said memory cell block and a signal for further halving said memory cell block; and

a second construction wherein the selection signal of said third gate is generated from a gate selection signal of said select transistor.

34. (Original) A semiconductor integrated circuit device according to claim 30, which has any of the following constructions:

a first construction wherein contact holes are disposed at said bundling portion of said third gates; and

a second construction wherein said third gate and said dummy gate are connected through a contact hole and a metal wire.

35. (Original) A semiconductor integrated circuit device according to claim 31, wherein:

said third gate is formed as it is buried into the space between said first gates extending in a direction vertical to said word line; and

a decoder for driving said third gate is disposed in an extending direction of said word line.

36. (Original) A semiconductor integrated circuit device according to claim 35, which has any of the following constructions:

a first construction wherein said decoder for driving said third gate is disposed at one of the ends of said memory cell array;

a second construction wherein said decoder for driving said third gate is disposed adjacent to a block decoder for selecting said memory cell block; and

a third construction wherein said decoders for driving said third gate are so disposed on both sides of said memory cell arrays as to interpose said memory cell array between them, adjacent to said block decoder for selecting said memory cell block.

37. – 112. (Cancelled)